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HIP-14-050

14
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Project Title

Coarse Grain Simulations of RDX Using DPD-RX: Effects of Interfaces and Voids

Includes:
Title line,
Authors with
Affiliation

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HIP Intern as first
author, followed
by Mentor, then
any others you
and your mentor
would like to add

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ABSTRACT
Single paragraph
approximately
250 words

Abstract

This research project was conducted at Wright Patterson Air Force Base in Dayton, OH. The goal of the project was to see what happens at a liquid-vacuum interface when a surfactant molecule is added to water. Using the molecular dynamics software LAMMPS (Large-scale Atomic/Molecular Massively Parallel Simulator), the interface with the surfactant SDS in water was simulated. Using a `pizza.py` script, the density of each atom type was calculated and plotted. I wrote parallel code that calculates the center of mass and dipole moments of each molecule at each time-step, in addition to calculating six different autocorrelation functions. These results were plotted and animated so that one can visualize what is happening at the interface. The plots show that the surfactant molecules go to one end of the interface, with the bulk being almost all water. The carbon tail of the surfactant was outside the interface, while the head is inside the interface, which was indicated by the density plot and the dipole moment calculations.

INTRODUCTION

Goals and purpose of project

INTRODUCTION (continued)

Can be labeled "Introduction" or "Project Objectives"

MATERIALS and METHODS

Can be labeled "Materials and Methods", "Experimentation and Analysis", "Methodology", etc.

You can imbed your figures, charts, and graphs in the body of this section, or you can put them at the end of the paper, either is acceptable within the confinement of maximum page length.

Introduction

With the projected development of the future battlespace comes a new set of requirements for hardware to better suit this space. The new battlespace will feature increasingly contested environments, in some cases denied to joint military forces, which will necessitate alternate approaches to processing, exploitation, and dissemination (PED). The approaches will have to shift from permissive intelligence, surveillance, and reconnaissance (ISR) domains to non-permissive domains which are referred to as non-traditional ISR(NTISR). These new approaches will require that the hardware, utility of embedded processing architectures, will be driven by energy-efficiency as much as high performance. This is relevant to this project as it is unknown whether or not these processors meet the above requirements therefore we must test specific benchmark applications for performance and power efficiency. The goal of this project is to evaluate, using a set of kernels/applications, the performance and power consumption on two emerging high performance energy efficient embedded computing (HPEEC) processing architectures.

Materials and Methods

There are numerous pieces that are poured into the creation of this system a webpage, daemon, three sets of staging algorithms, and a vast amount of computing nodes are required. The instantiation of a seamless, interactive system begins with the user interface. In this scenario, the user interface, written in PHP, HTML and CSS is a web page where biologists are directed for creating an EBR (electronic batch record). There are multiple configurations that can be entered, such as different algorithms to be used, as well as various cell types and infections to be chosen and added. After a biologist makes an EBR with the developed web portal, it is then submitted for analysis and backed up in a MySQL database. This process is accomplished by dynamically creating a configuration file and placing it into a specified directory from which the daemon will pull. The daemon, a piece of software written in Python that continually runs in the background, constantly searches for these files to appear. Once it sees a file generated by the web portal, it turns it into a zip file and packs the configuration file, a python wrapper script, and a program that does some analysis. At this point, user interaction is no longer required. The daemon then, programmatically, submits the zip file with parameters explicitly defined, based on what was previously entered in the EBR, to an instance of MindModeling using XMLRPC. Once in MindModeling, the job is verified and sent out for stage one analysis in parallel amongst many nodes in a supercomputer. While work is being done, the daemon monitors the progress of everything and updates the web portal accordingly by executing MySQL queries. After an analysis algorithm has finished, the daemon notices this and prepares it for stage two submission. Again, the same zipping procedure is approached, and after pushing the file out for analysis, the daemon goes back to monitoring the status of jobs in the system. This process happens one last time for stage three, and after this the

daemon takes the computed results and zips them up for the user. The user, also, has the ability to abort the process if there is uncertainty or unhappiness with the results being returned at any point. All of the components built by the students are written using the VI editor, and the git version control system is also used to help each other collaborate and keep up to date with newer versions created.

Results

The project is in the development phase and values are being tested on a larger scale, the final imaging scene. The project started with the Cornell box with the participating medium and now the program renders the participating medium in the ocean scene. Additional testing will allow for realistic depiction of optical thickness and distribution functions for the optical thickness. Further implementation will allow for power and area values for the laser as well as the sun background signal. Figure 4 shows the final result of rendering a laser scattering in fog. It was generated on a 32 core HPC machine. These initial results look promising and show that the careful project testing and development process developed works well and can produce quality images. What remains is the validation that the physical numbers generated indeed make physical sense. In the end, robust and flexible testing and development process has been developed, which will make future work seamless and require less effort.

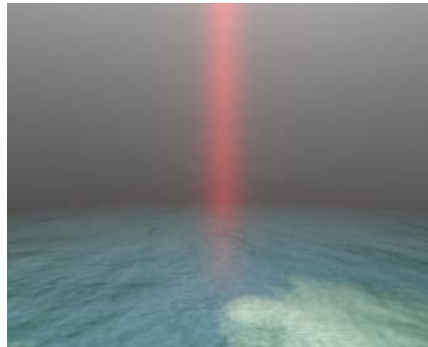


Figure 4. Final Rendering Result. This image shows a laser scattering in an isotropic fog in the same ocean scene as in Figure 3a.

Conclusions

Comparatively the Parallella is not as powerful as other boards in terms of performance yet the Parallella uses far less power. This is because $\text{energy-efficiency} = \text{performance}/\text{power}$ and the less power that is used the greater the efficiency. Also comparatively other boards might be easier to implement to

avoid the overhead of time lost spent trying to get the boards working properly. Knowledge gained from this experience includes: expanded Linux knowledge and toolset, increased awareness of the importance of technology that supports the warfighter, furthered education in system administration and server maintenance and developed better project management skills and experience.

Future work of the project includes finding a suitable benchmark to test for the maximum processing threshold of the Parallella in terms of processing capability and energy-efficiency. The OpenCL to STDCL conversion table will also need to be fully completed to ensure smoother transitions of OpenCL programs to STDCL. The CARMA is also being discontinued in this project due to the CARMA boards decommissioning and because of this the configuration issues encountered in the project were never fully resolved due to this pending transition. Instead, the NVIDIA Jetson boards are being considered and will be evaluated in place of the now decommissioned CARMA boards. The Jetson TK1 board features: Kepler GPU with 192 CUDA cores, 4-Plus-1 quad-core ARM Cortex A15 CPU, 2 GB x16 memory with 64 bit width, 16 GB 4.51 eMMC memory. Finally, the Parallella and now Jetson boards will need to be field tested in the applications necessary for the future battlespace to ensure field-usage is accurate to lab testing and results.

Impact of Summer Research Experience

Background

I am a PhD candidate at the University of Cincinnati in Electrical Engineering. I earned my MS from the same. For my thesis, I was introduced to NVIDIA's CUDA, a parallel programming language for General Purpose computing on Graphics Processing Units (GPGPU). CUDA is an extension of the C computing language, though the compiler allows for some C++ data structures. Although I had very limited programming experience in my undergraduate coursework, I taught myself C++, MATLAB, and Python during the first few years of graduate school, and have become fairly comfortable with them. I also have been a Windows-only user until this summer. I took part in the High Performance Computing Internship Program (HIP) with the goals to improve my high performance computing (HPC) knowledge and skills, contribute to a professional research team, and expand my academic and professional network while on base.

Impact

The HPC internship program was an incredibly educational and rewarding experience for me. When I first began this internship in May I had very little knowledge of chemistry and had no idea what molecular dynamics was, and had never wrote any parallel programs before. I have also never had to deal

IMPACT OF
SUMMER
RESEARCH
EXPERIENCE
(continued)

with optimizing algorithms to run more quickly and use less memory. Now, at the end of the summer, I feel confident about writing parallel programs and have a much greater understanding of molecular dynamics and how it relates to heat transfer. This internship will make me consider speed and memory use while coding, instead of just using the simplest implementation. I greatly appreciate Dr. Eugeniya Iskrenova-Ekiert for helping me learn how to submit jobs to the pbs queue and how to install and use MPI. I had Linux experience before this internship, but had not submitted jobs to a pbs queue or used MPI, and feel that I will use MPI in the future. One of my favorite things that I learned in my ten weeks here was MPI. In school, all of the programs I would write for class would run on only one core. MPI was very interesting because it allowed me to use many processors and write my code in a different style than I would if it were to be serial code. My first attempts to use MPI made the code take much longer than its serial counterpart and sometimes even ran out of memory. Once I started to get the hang of MPI I was able to make the code run much faster and manage memory much better. I feel very lucky that I was chosen for this opportunity to conduct research. I found it to be a very eye-opening experience, as I have never worked in research before and it was very interesting seeing what working in the real world is like. This internship has taught me a great deal about how to be a researcher and has already opened the door to new opportunities.

Acknowledge-
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